Amendments to the Claims:

1. (Previously presented) A system comprising:

N different memories wherein N> 1;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode; and

a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories.

2. (Previously presented) The system of Claim 1 wherein the at least first mode includes a Read mode.

3. (Previously presented) The system of claims 1 or 2 wherein each of the N different memories includes DDR DRAM.

4. (Previously presented) The system of claim 3 wherein each of the DDR DRAM is partitioned into at least four banks and at least one buffer is spread across the at least four banks.

5. (Currently Amended) ~~The system of claim 4~~ A system comprising:

N different memories wherein N> 1 and each of the N different memories includes DDR DRAM partitioned into at least four banks and at least one buffer spread across the at least four banks;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode; and

a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories, wherein the at least one buffer is partitioned into multiple maskable units.

6. (Previously presented) ~~The system of claim 4~~ A system comprising:

N different memories wherein N> 1 and each of the N different memories includes DDR DRAM partitioned into at least four banks and at least one buffer spread across the at least four banks;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein

said each one of the plurality of memory controllers setting an associated different memory in at least a first mode; and

a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories, wherein the at least one buffer is partitioned into four units.

7. (Previously presented) The system of claim 6 wherein each unit is equivalent to 1/4 the size of the at least one buffer.

8. (Original) The system of claim 6 wherein each unit is maskable.

9. (Currently Amended) ~~The system of claim 1 further including~~ A system comprising:

N different memories wherein N> 1;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode;

a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories

set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories; and

a controller operatively coupled to said arbiter, said controller executing a selection algorithm to select one of the N different memories in which data is to be written said selection algorithm comprising:

- Exclude slices scheduled for re-fresh cycle (indicated by each DRAM controller)
- Assign slices for all R requests of Transmitter controller
- Complement R-accesses from corresponding EPC queue [Slice; QW]
- Assign slice to EPC for globally W excluded slices (e.g. slice is excluded by all slice exclusion rules from Receiver)
- Assign slices to W requests in RR (Round Robin) fashion between non-excluded slices staring from last assigned slice (slice assigned to Receiver Controller in previous window)
- Complement W-accesses by EPC accesses from corresponding EPC queue [Slice; QW] and
- Assign slice to EPC requests according to priority expressed by Weight.

10 - 23. (Canceled)

24. (Previously presented) A method comprising:

providing a plurality of separate memory elements in which frames from communication device are to be stored or retrieved;

partitioning at least one of the frames with a controller into at least two parts;

storing each one of the at least two parts into different ones of the plurality of separate memory elements; and

providing a single arbiter responsive to a request signal to cause the different ones of the plurality of separate memory elements to be read simultaneously wherein each one of the adjoining parts is available simultaneously on respective busses associated with each of said ones of the plurality of separate memory elements.

25. (Previously presented) A method including:

providing a plurality of separate memories in which data is stored;

providing a single arbiter to grant access to the plurality of separate memories;

receiving in the single arbiter a request to read data from selected ones of said plurality of separate memories; and

simultaneously reading said selected ones of said plurality of separate memories to provide data simultaneously on individual busses coupled to the selected ones of said plurality of separate memories.

26. (Previously presented) The method of claim 25 wherein the bandwidth of data on each one of the individual busses is less than the total bandwidth on all activated busses.

27. (Previously presented) A method comprising:

providing a plurality of separate memory modules in which frames are being stored;

partitioning a frame into multiple parts;

writing adjacent parts of the frame so partitioned in different ones of the plurality of separate memory modules; and

simultaneously accessing, with a single arbiter, multiple ones of the plurality of separate memory modules in a single memory access window to

read data therefrom wherein the total bandwidth of data output from the multiple memory modules matches the bandwidth of a FAT pipe port associated with a communication device.

28. (Currently Amended) ~~The system of claim 9 wherein the controller includes~~ A system comprising:

N different memories wherein N> 1;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode;

a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories; and

a controller operatively coupled to said arbiter, said controller executing a selection algorithm to select one of the N different memories in which data is to be written said selection algorithm comprising:

- Exclude slices scheduled for re-fresh cycle (indicated by each DRAM controller)
- Assign slices for all R requests of Transmitter controller
- Complement R-accesses from corresponding EPC queue [Slice; QW]

- Assign slice to EPC for globally W excluded slices (e.g. slice is excluded by all slice exclusion rules from Receiver)
- Assign slices to W requests in RR (Round Robin) fashion between non-excluded slices staring from last assigned slice (slice assigned to Receiver Controller in previous window)
- Complement W-accesses by EPC accesses from corresponding EPC queue [Slice; QW] and
- Assign slice to EPC requests according to priority expressed by Weight, wherein the controller includes a state machine or other hardware circuits.

29 - 32. (Canceled)

33. [[32.]] (Currently Amended) A system comprising:

N different memory elements, N > 1, wherein at least two of said N different memory elements are each partitioned into multiple sectors and each of the at least two of said N different memory elements so partitioned is partitioned into at least one buffer spread across said multiple sectors;

a plurality of memory controllers with each one of said plurality of memory controllers operatively coupled to each one of the N different memory elements; and

a single arbiter operatively coupled to the plurality of memory controllers, said single arbiter being response to a write request signal to generate a write control signal that causes data to be written in one of the at least one buffer associated with one of the at least two of said N different memory elements.

34. (Previously presented) The system of claim 33 further including said single arbiter being responsive to a read request signal to generate a read control signal that

causes data to be read from another of the at least one buffer associated with another of the at least two of said N different memory elements.

35. (New) A system comprising:

N different memories wherein N> 1 and each of the N different memories includes DDR DRAM partitioned into at least four banks and at least one buffer spread across the at least four banks;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode including a read mode; and

a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories, wherein the at least one buffer is partitioned into multiple maskable units.

36. (New) A system comprising:

N different memories wherein N> 1 and each of the N different memories includes DDR DRAM partitioned into at least four banks and at least one buffer spread across the at least four banks;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode; and

a single arbiter responsive to at least one signal requesting access to the N different memories wherein said single arbiter generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories set in the at least a first mode wherein total bandwidth on selected ones of the M different busses of the N different memories is greater than the bandwidth on a single bus of the M different busses of the N different memories, wherein the at least one buffer is partitioned into four units.